

FIGURE 1 (PRIOR ART)

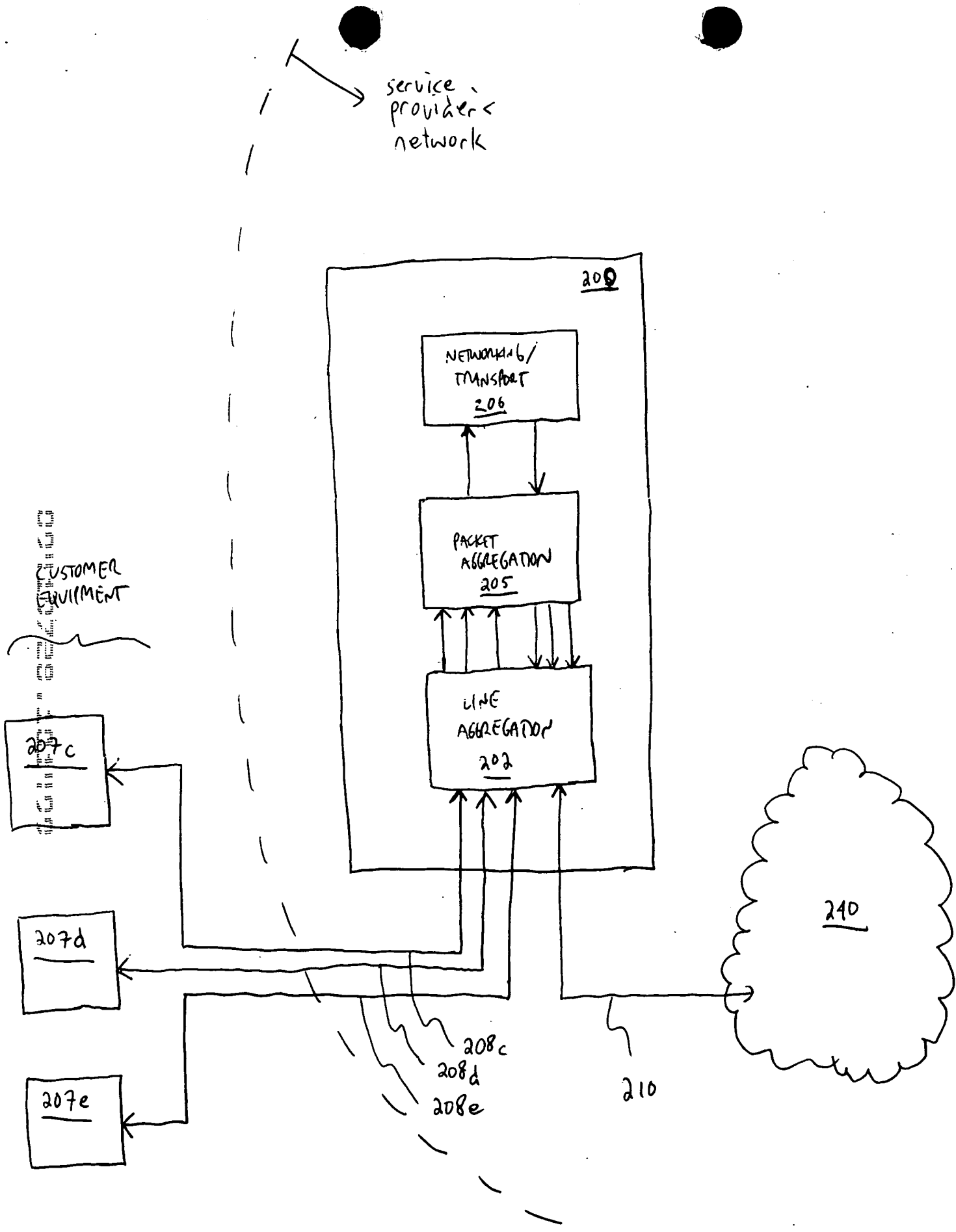


FIGURE 2A

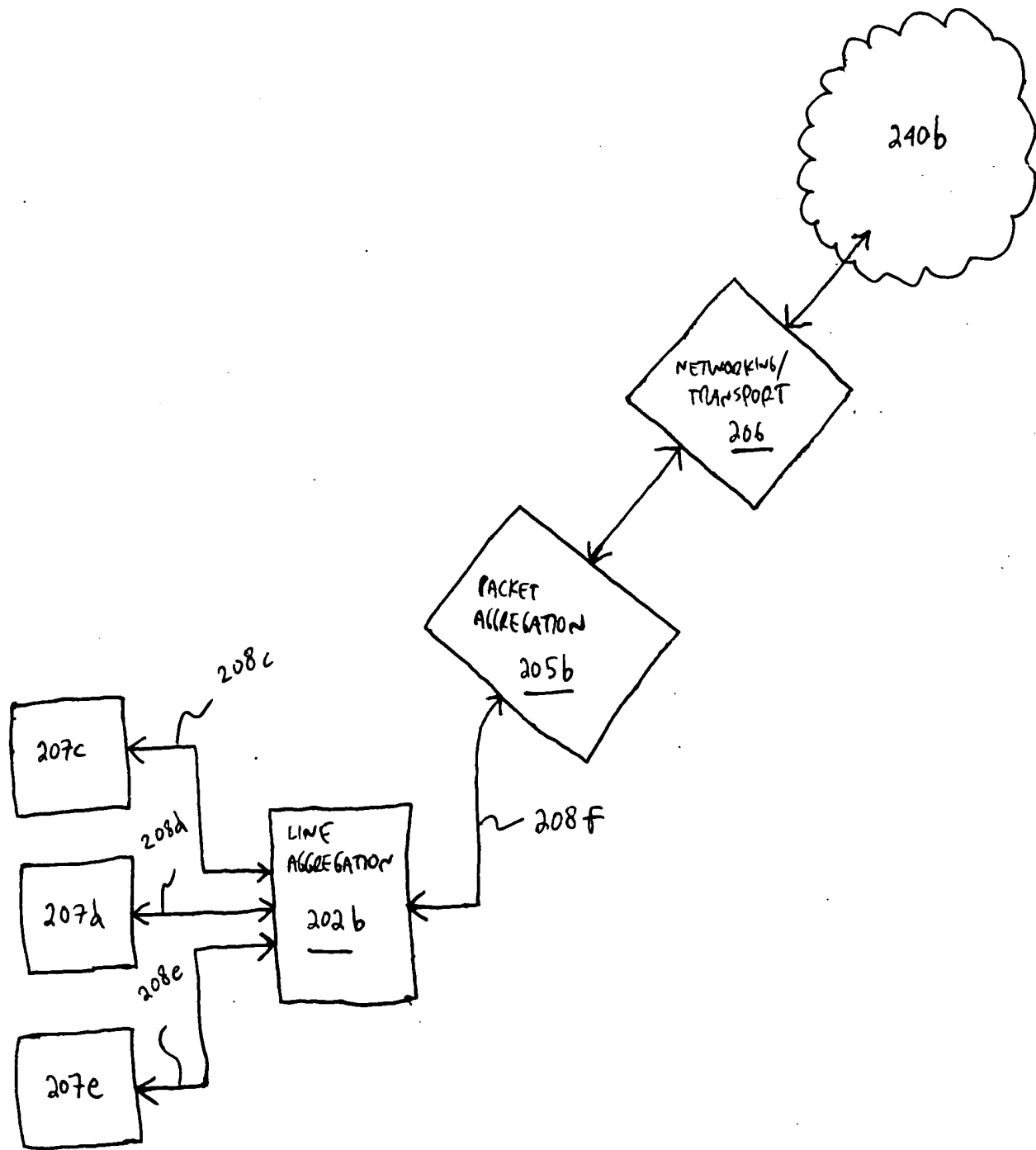


FIGURE 2b

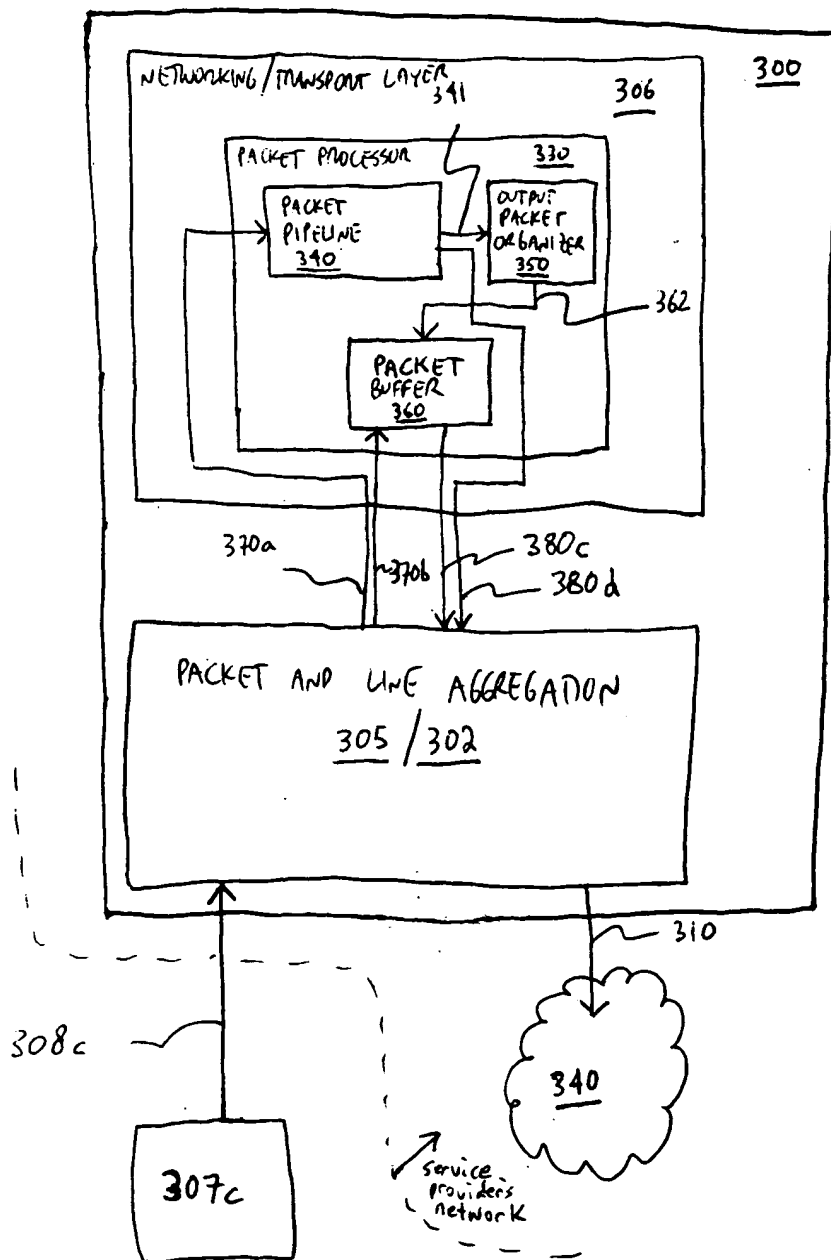


FIGURE 3A

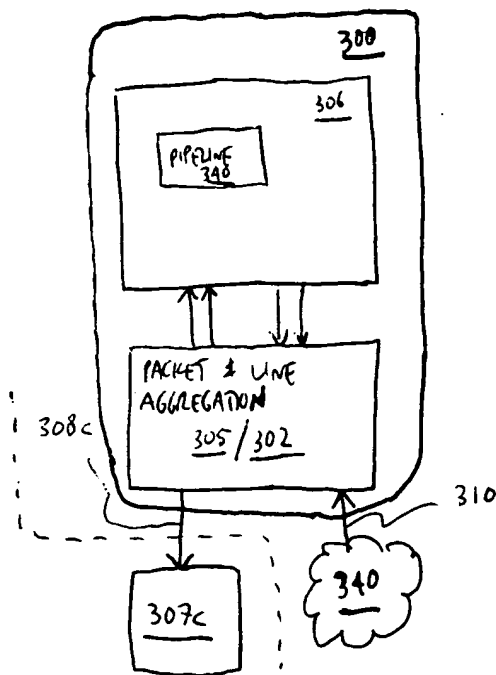


FIGURE 3B

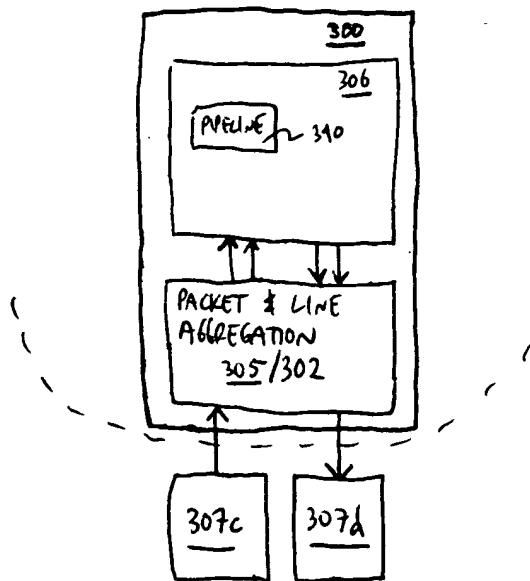


FIGURE 3C

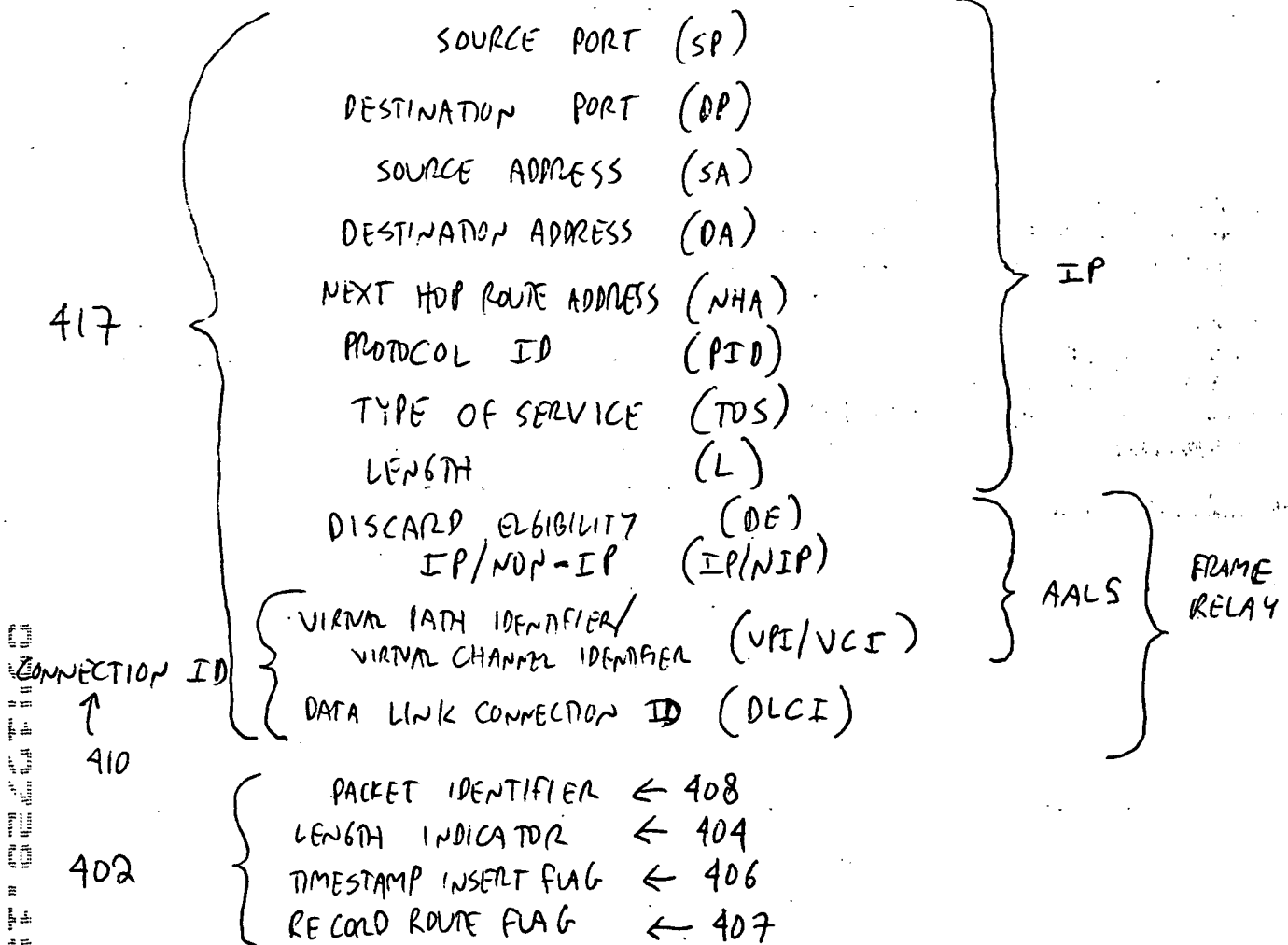


FIGURE 4

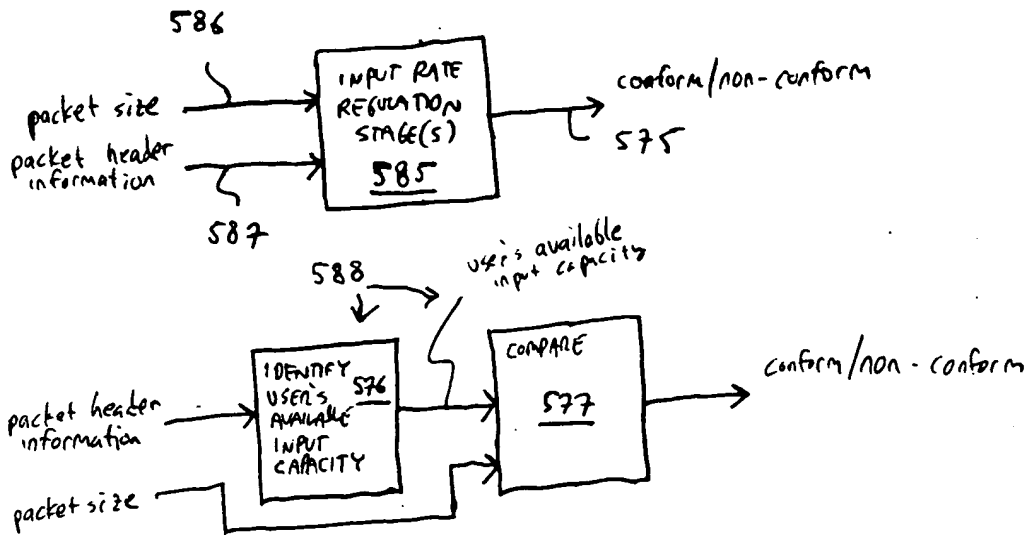


FIG. 5A

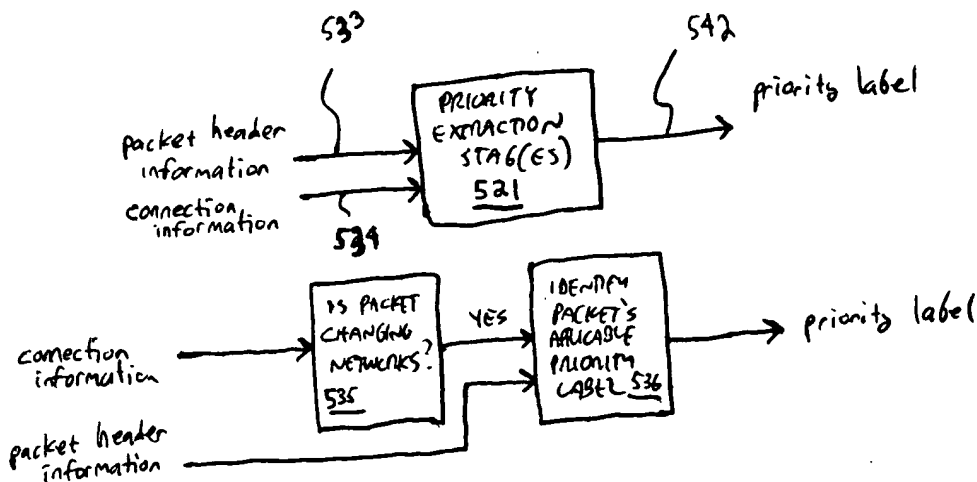


FIG. 5B

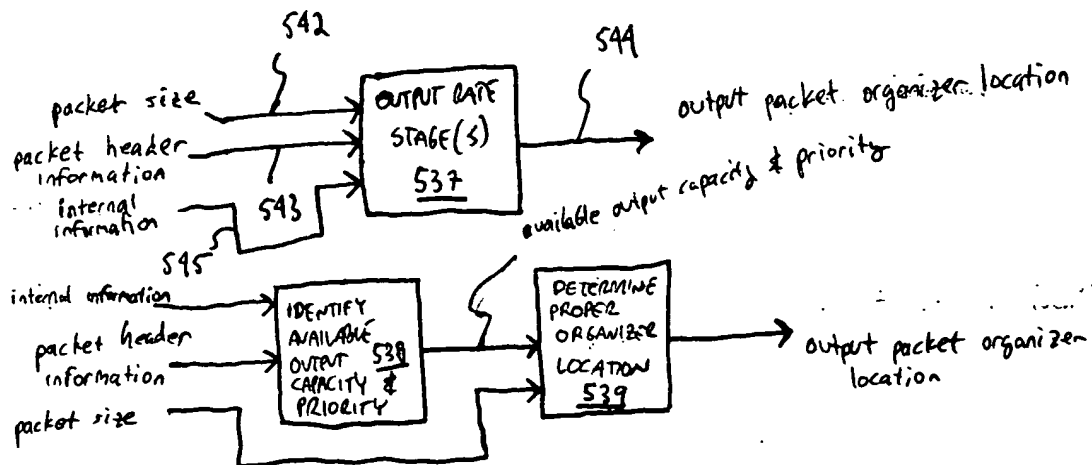


FIG. 5C

540

FIG. 5 is a block diagram of a packet scheduling system in accordance with the present invention.

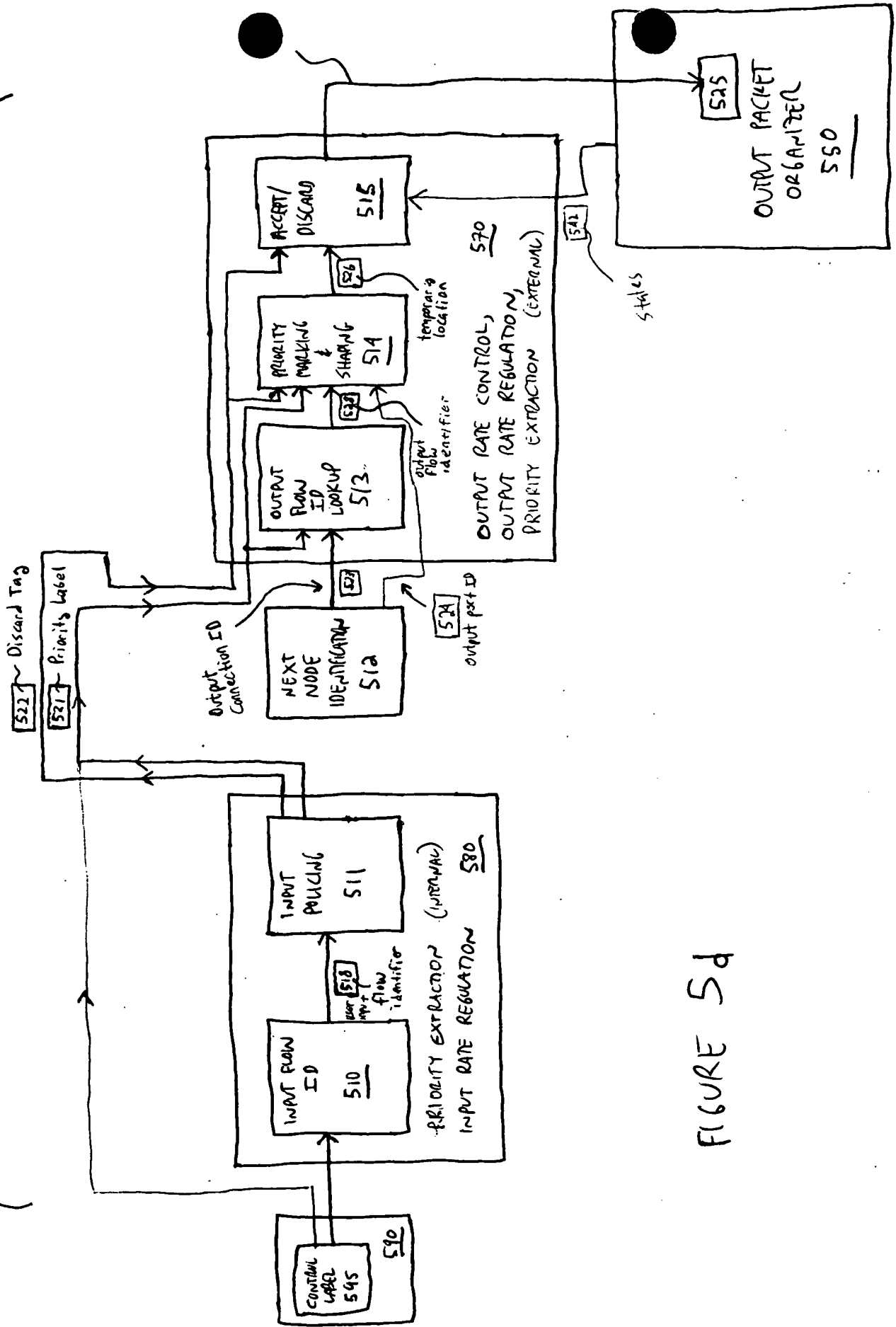


FIGURE 5d

FIG. 6A

INPUT FLOW ID STAGE	INPUT POLICING STAGE	NEXT NODE IDENTIFICATION STAGE	OUTPUT FLOW ID STAGE	PRIORITY MARKING AND SHARING STAGE	ACCEPT/DISCARD STAGE
------------------------	-------------------------	--------------------------------------	-------------------------	--	-------------------------

X	X	X		X	X
---	---	---	--	---	---

FIG. 6A

FIG. 6B

		X	X	X	X
--	--	---	---	---	---

FIG. 6C

X	X	X	X	X	X
---	---	---	---	---	---

FIG. 6D

		X		X	X
--	--	---	--	---	---

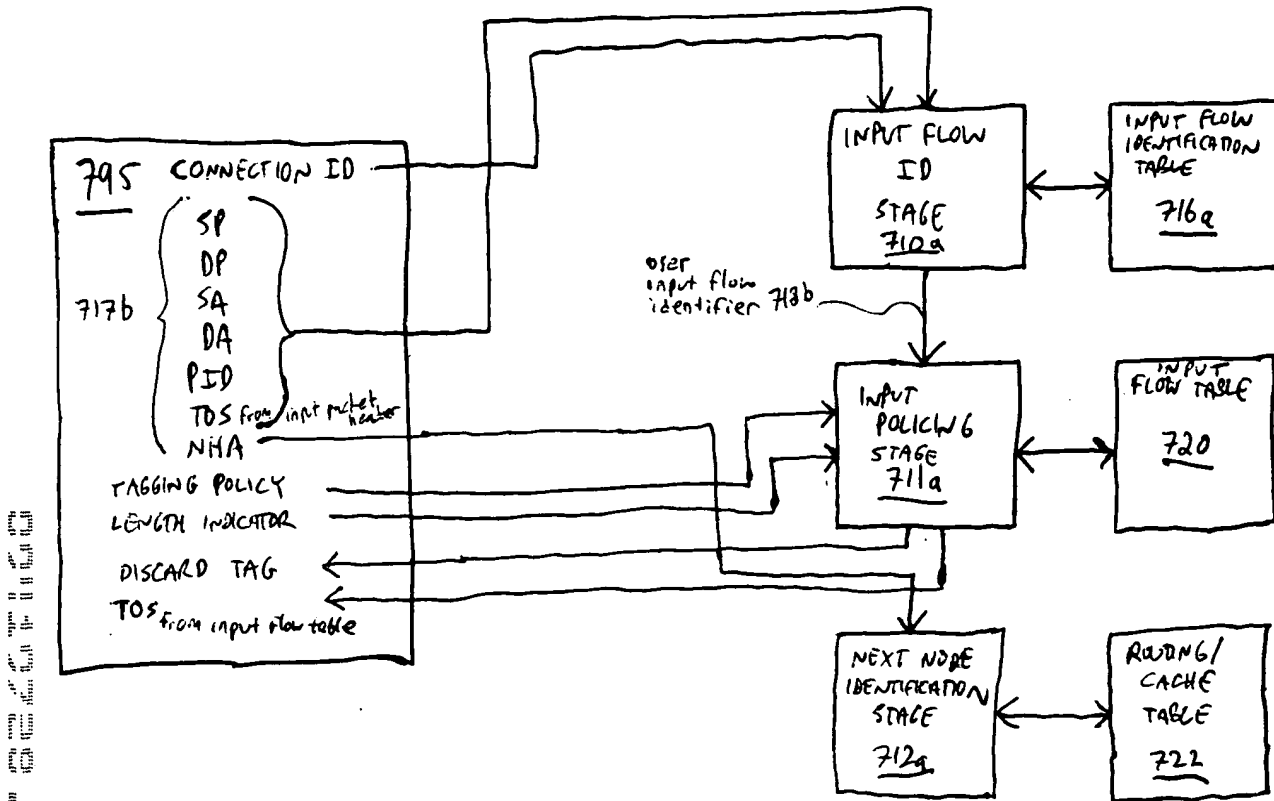


FIGURE 7A

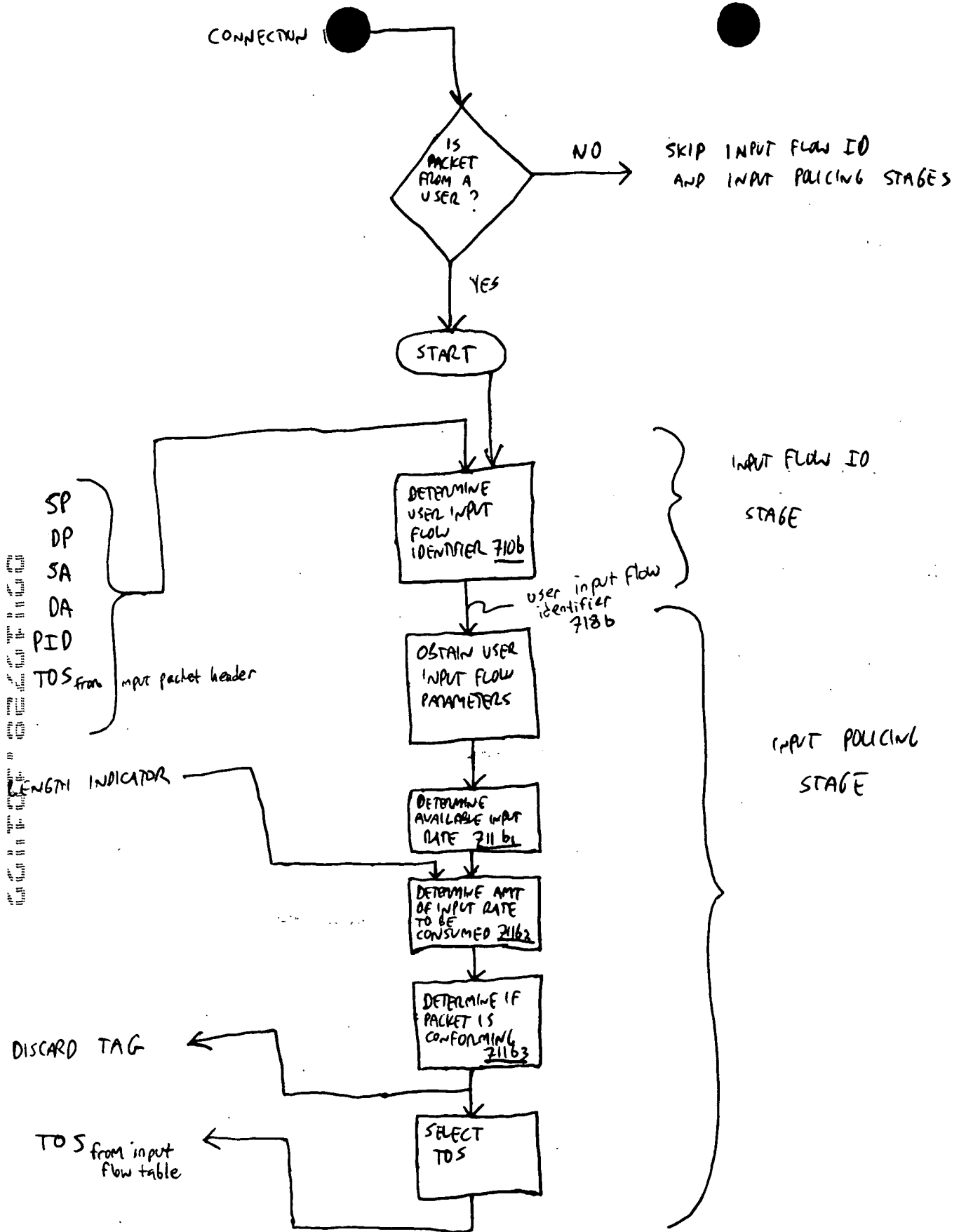


FIGURE 7B

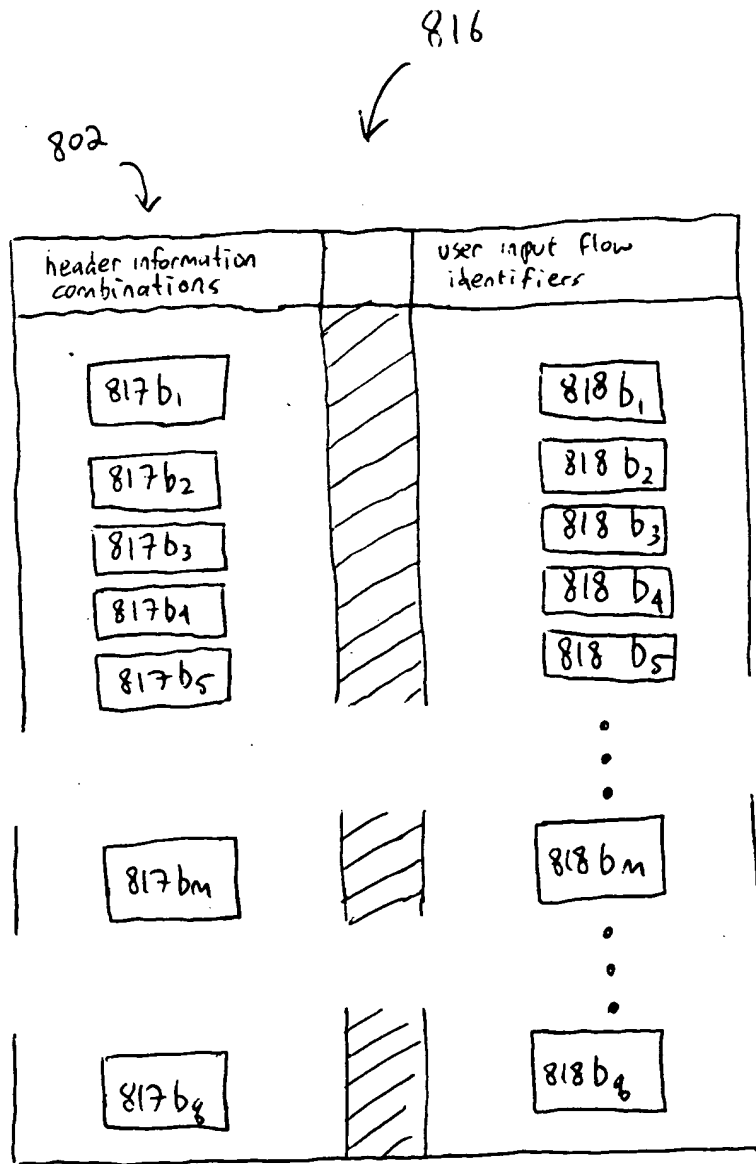
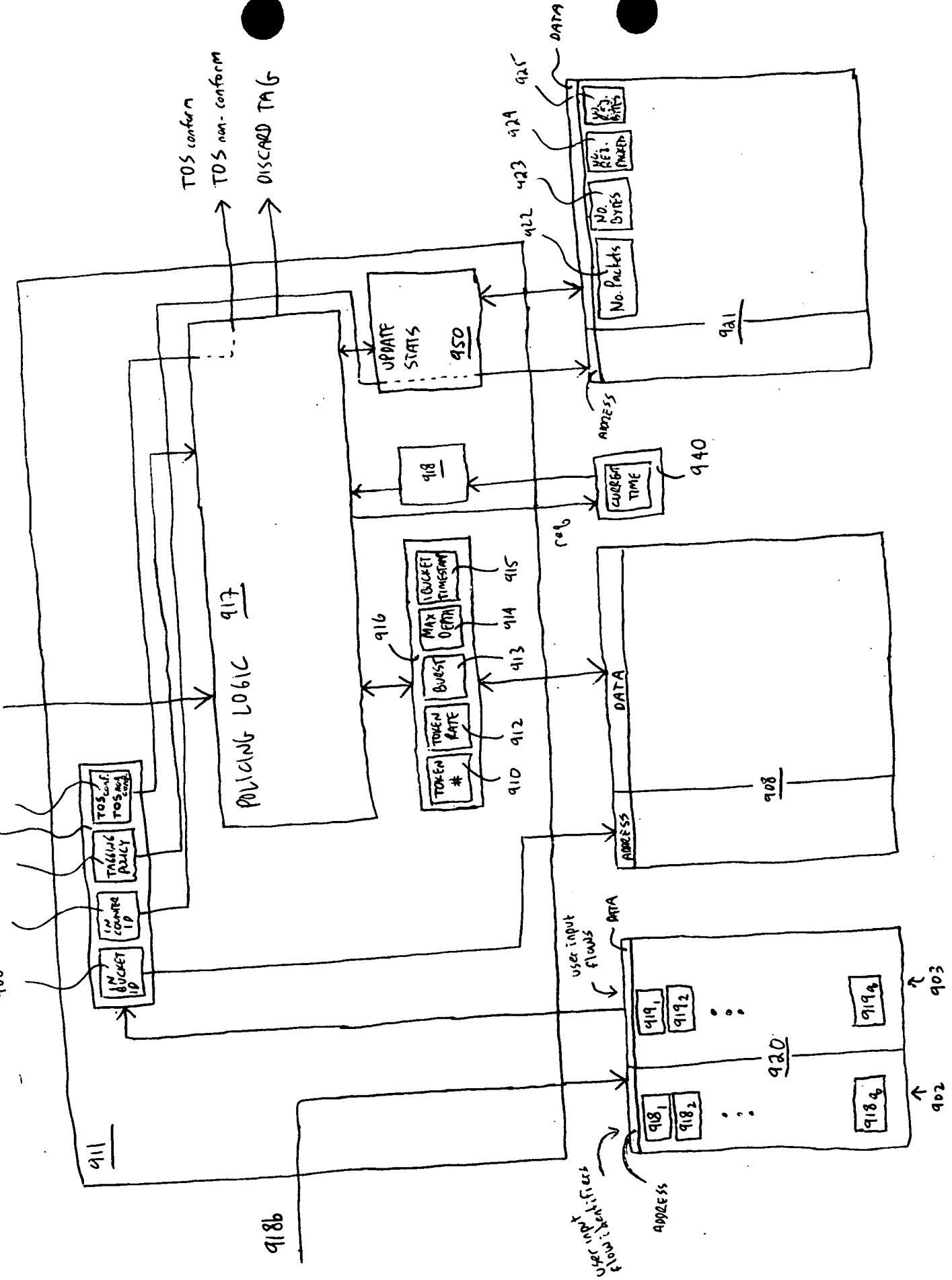


FIGURE 8

FIGURE 9

907
 906 909 904 905
 LENGTH INDICATOR



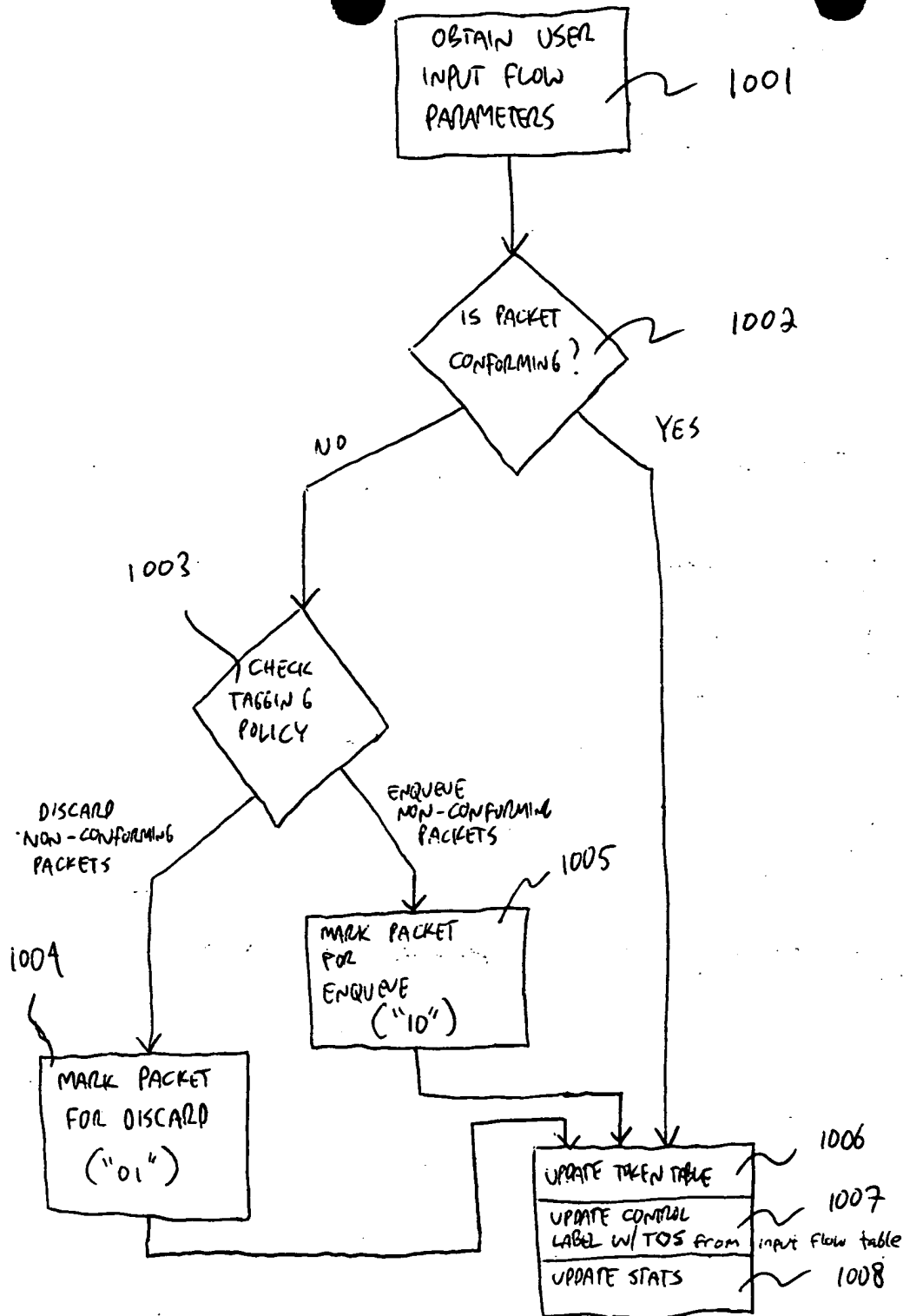


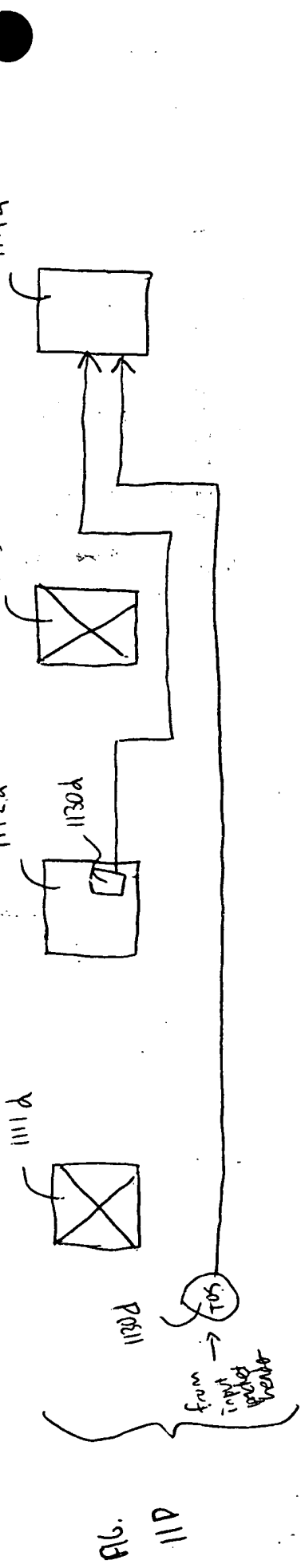
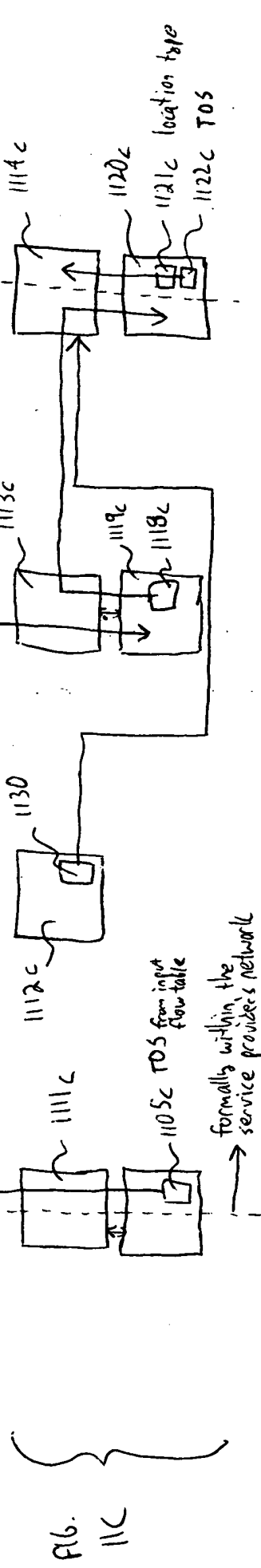
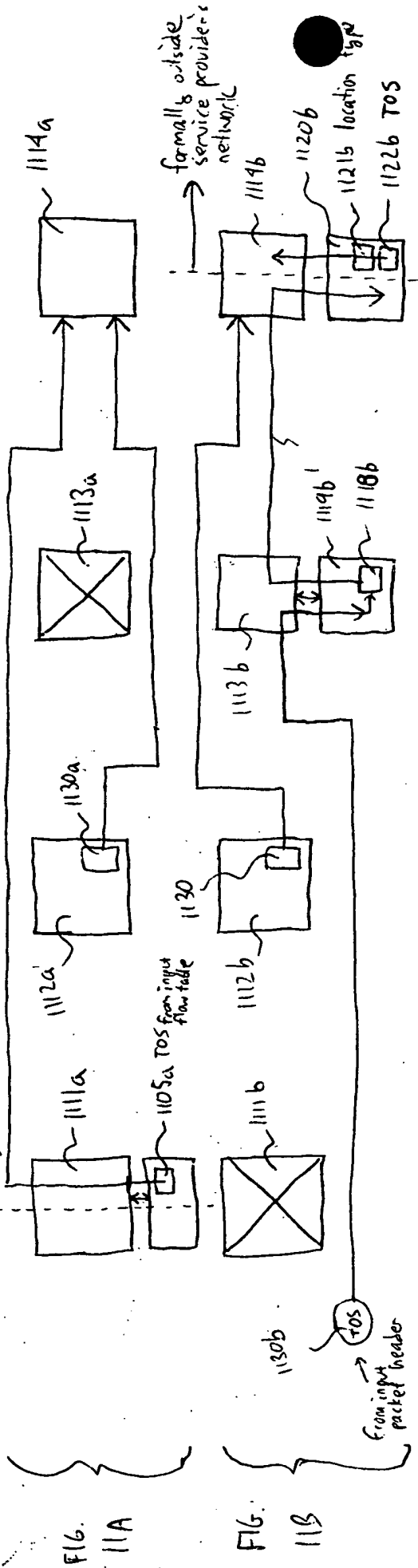
FIGURE 10

INPUT PUNCHING
STAGE

NEXT NODE ID
STAGE

OUTPUT FLOW ID
STAGE

MARKING / SHARING
STAGE



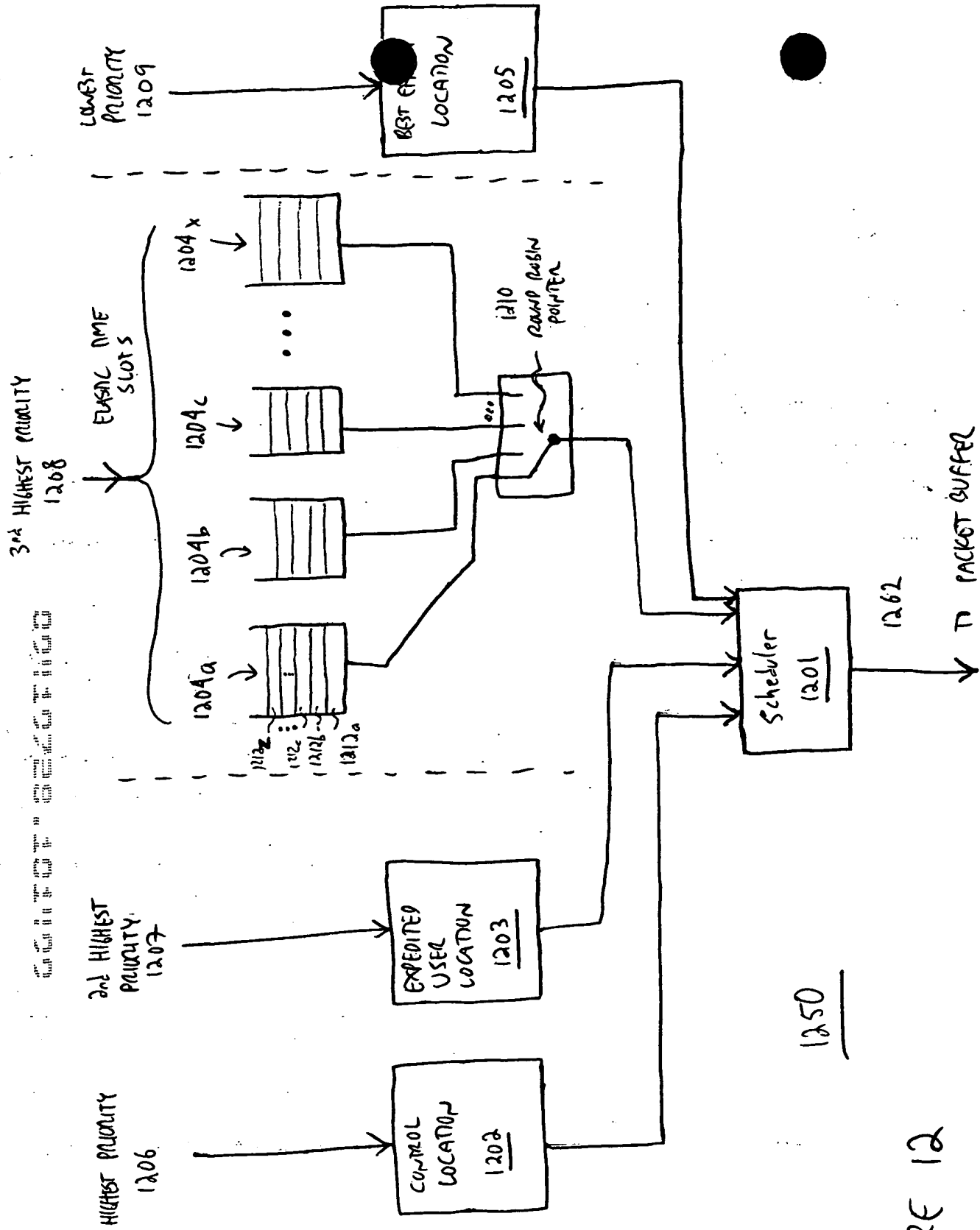


FIGURE 12

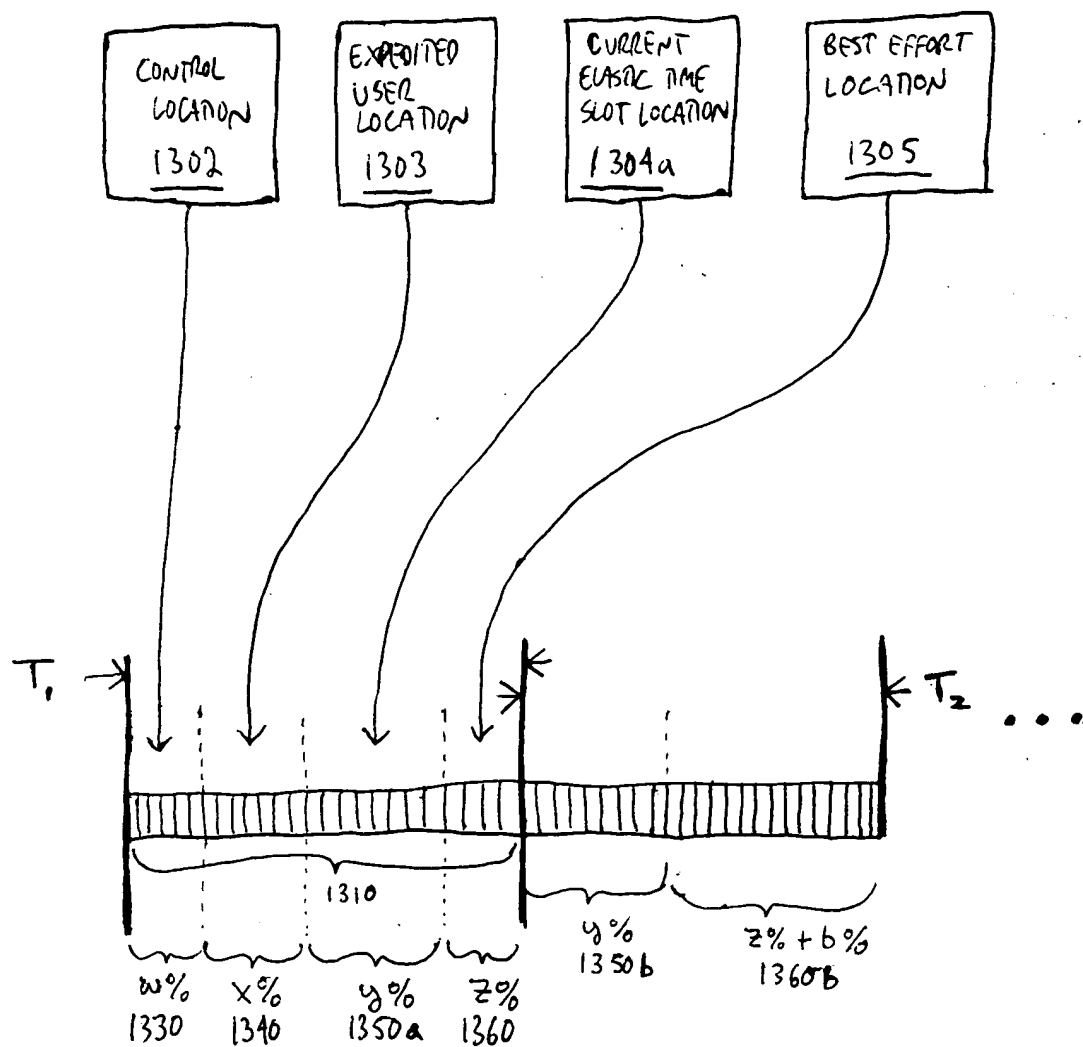


FIGURE 13

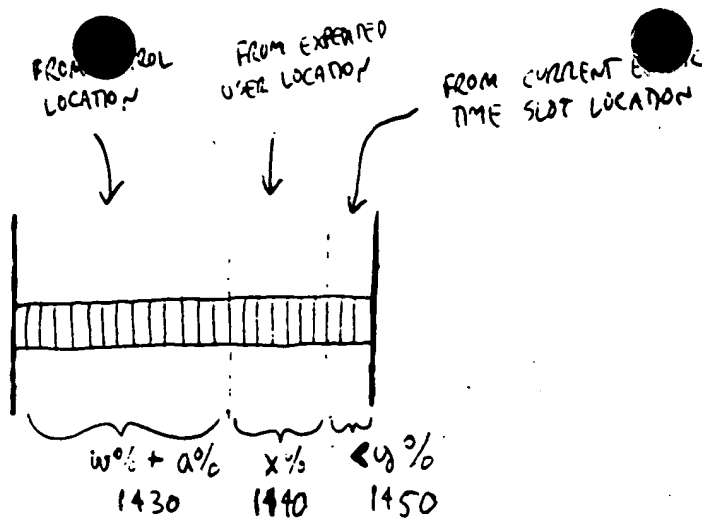


FIG. 14a

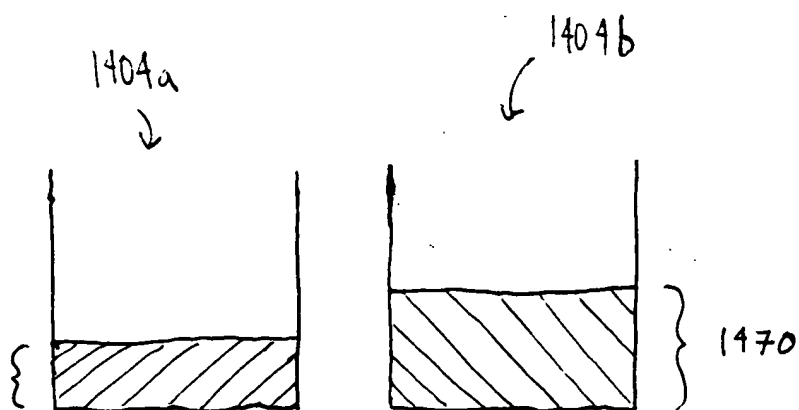


FIG. 14b

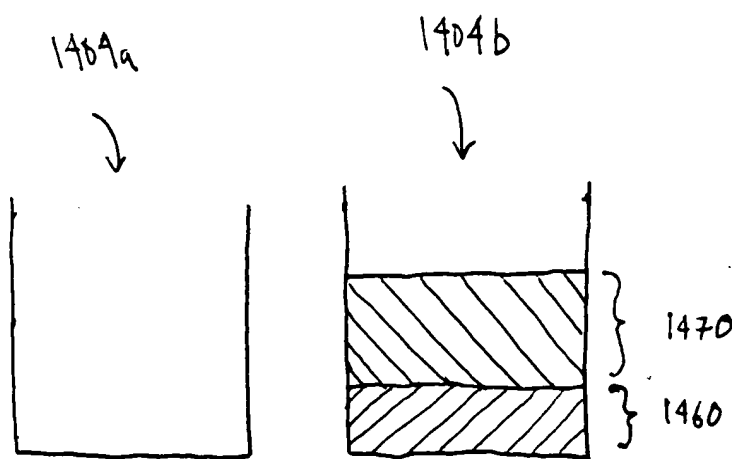


FIG. 14c

1500

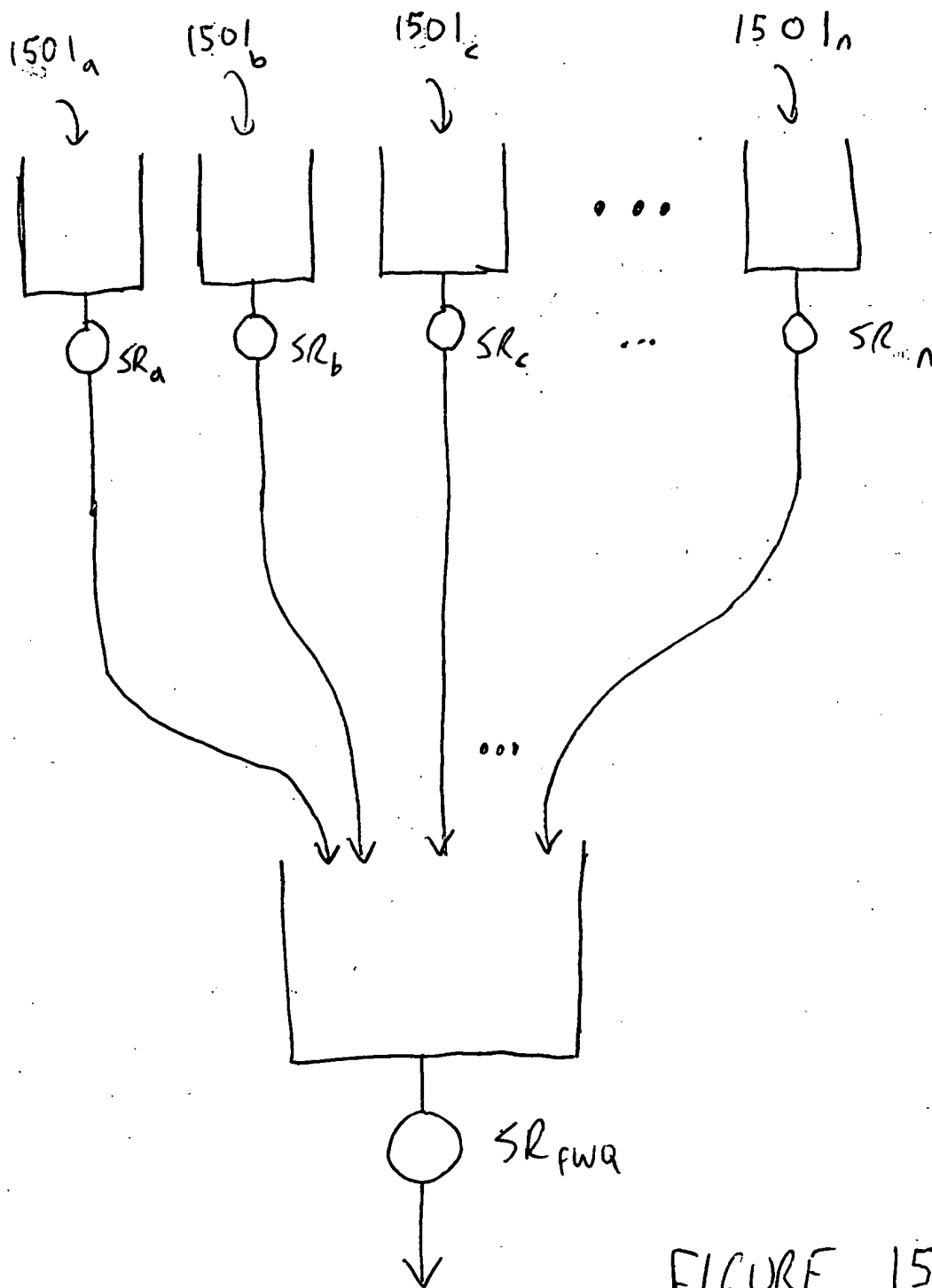


FIGURE 15

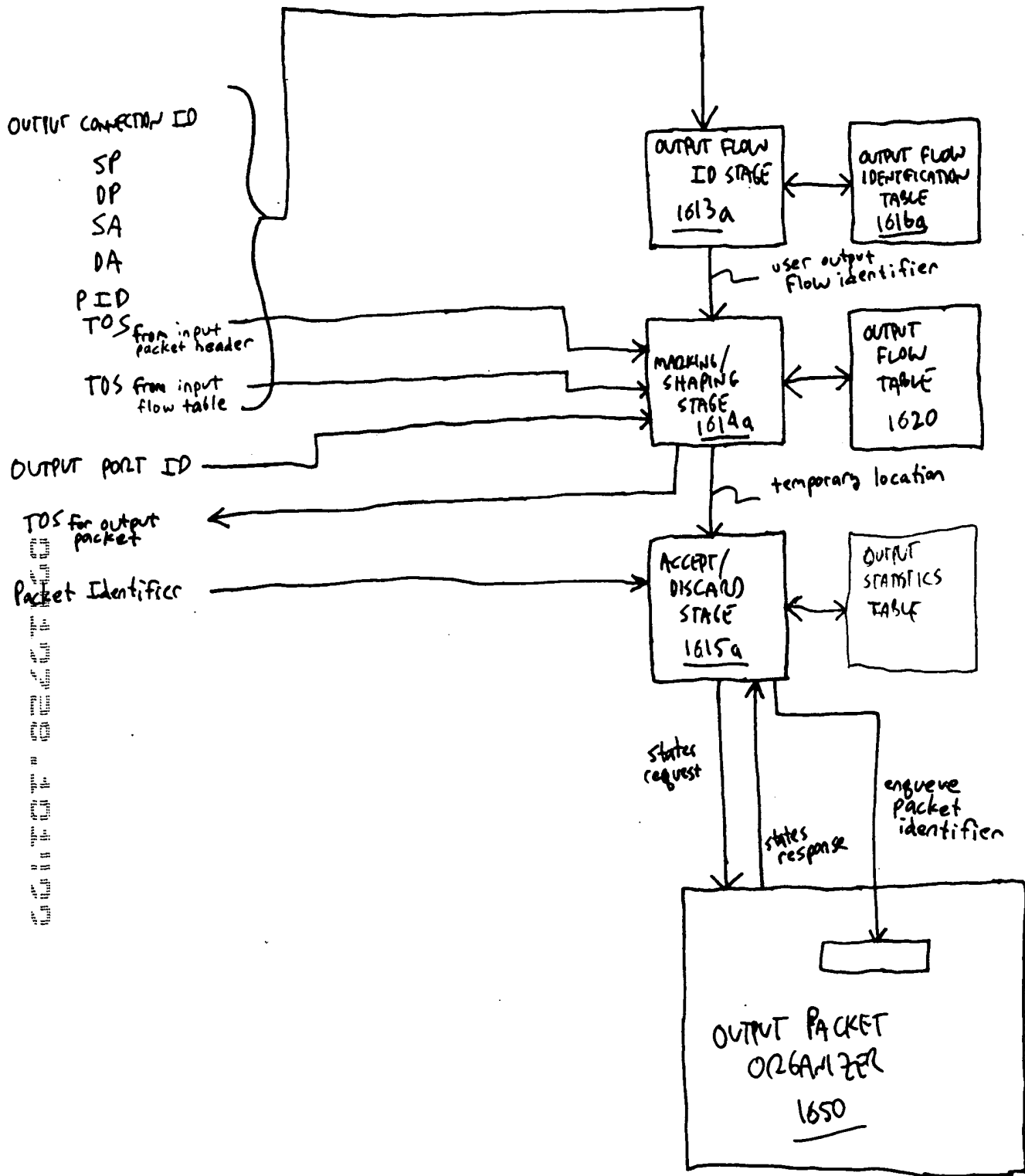
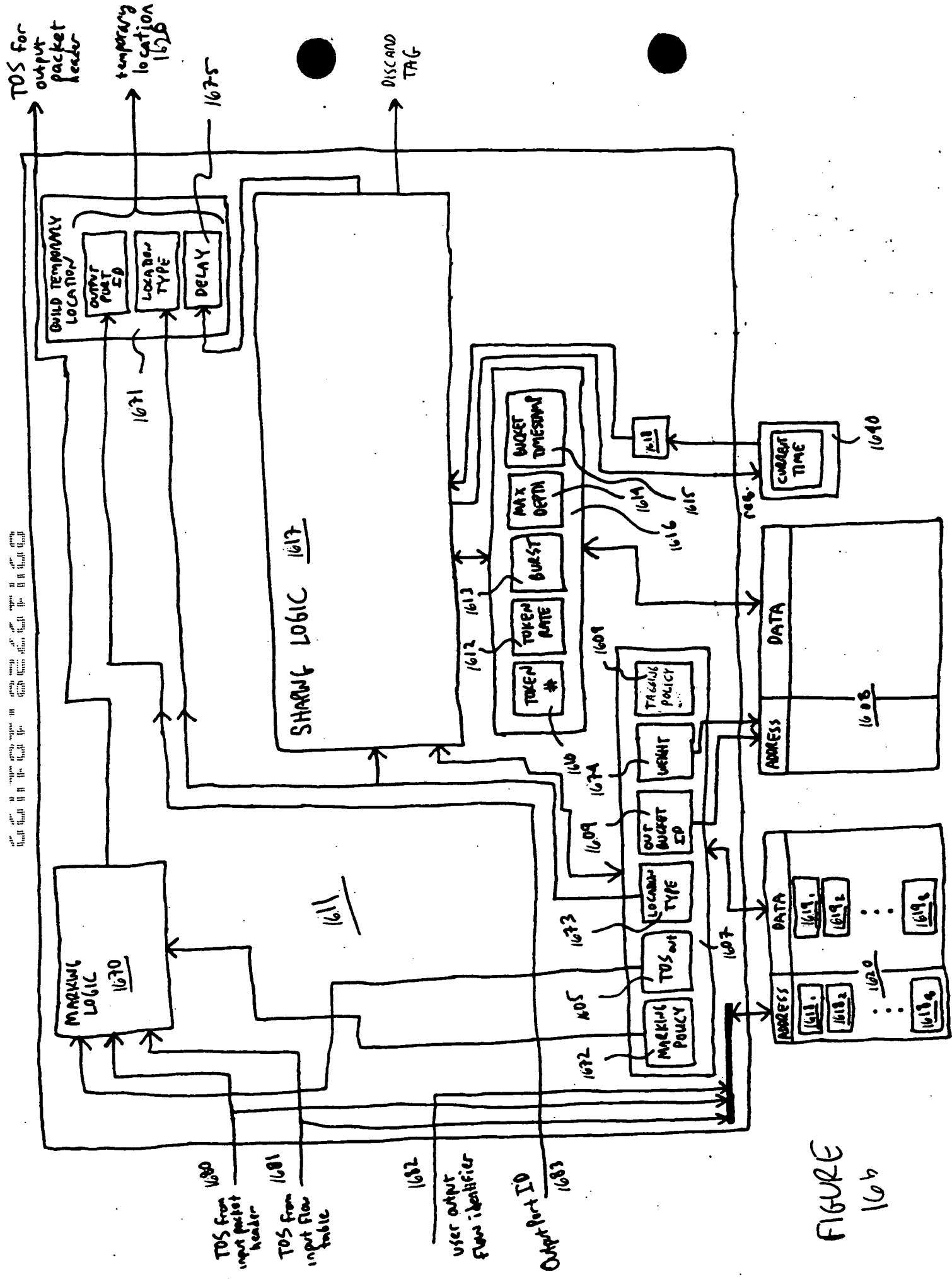


FIGURE 16_a



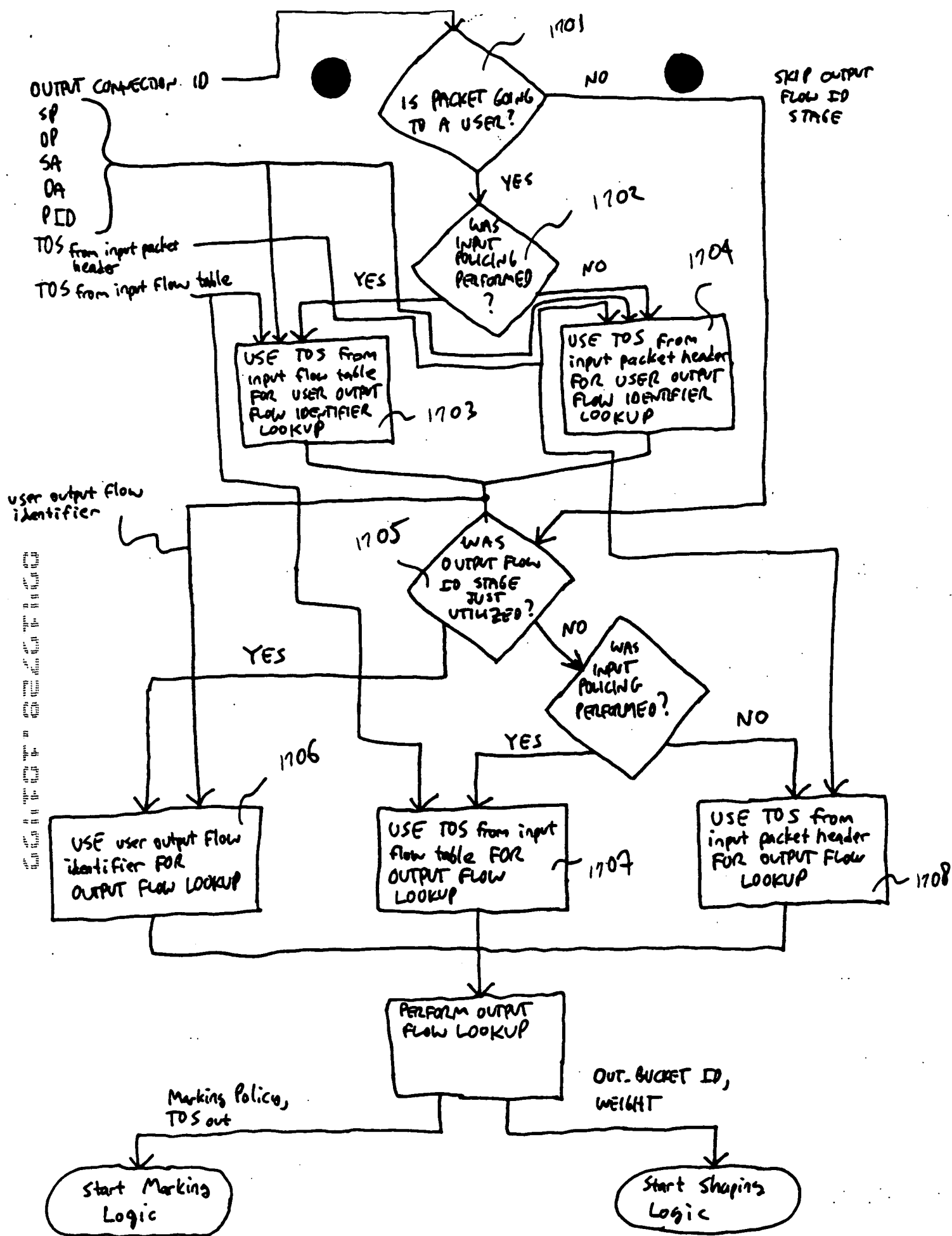


FIGURE 17a

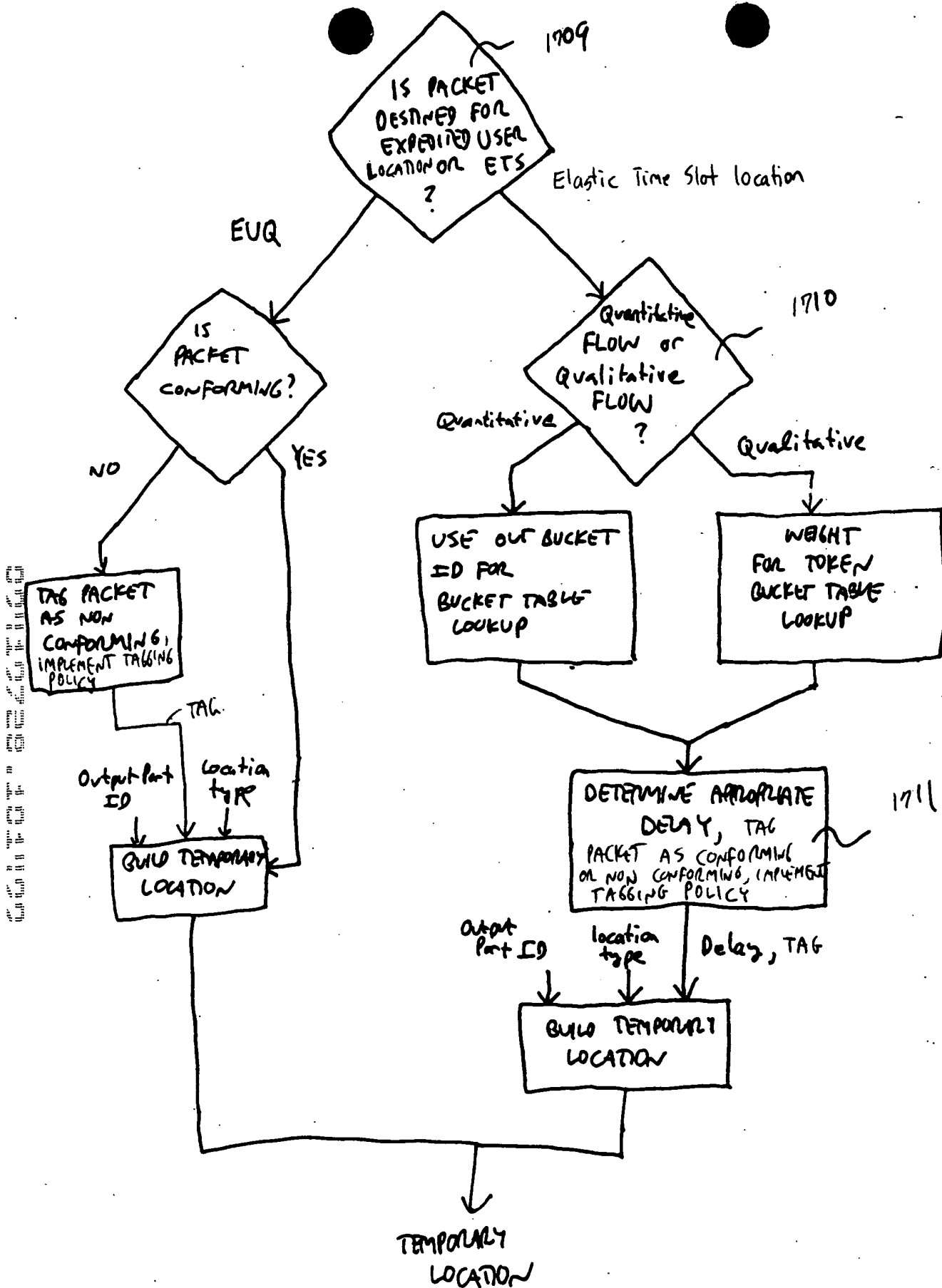


FIGURE 17b

Marking Logic

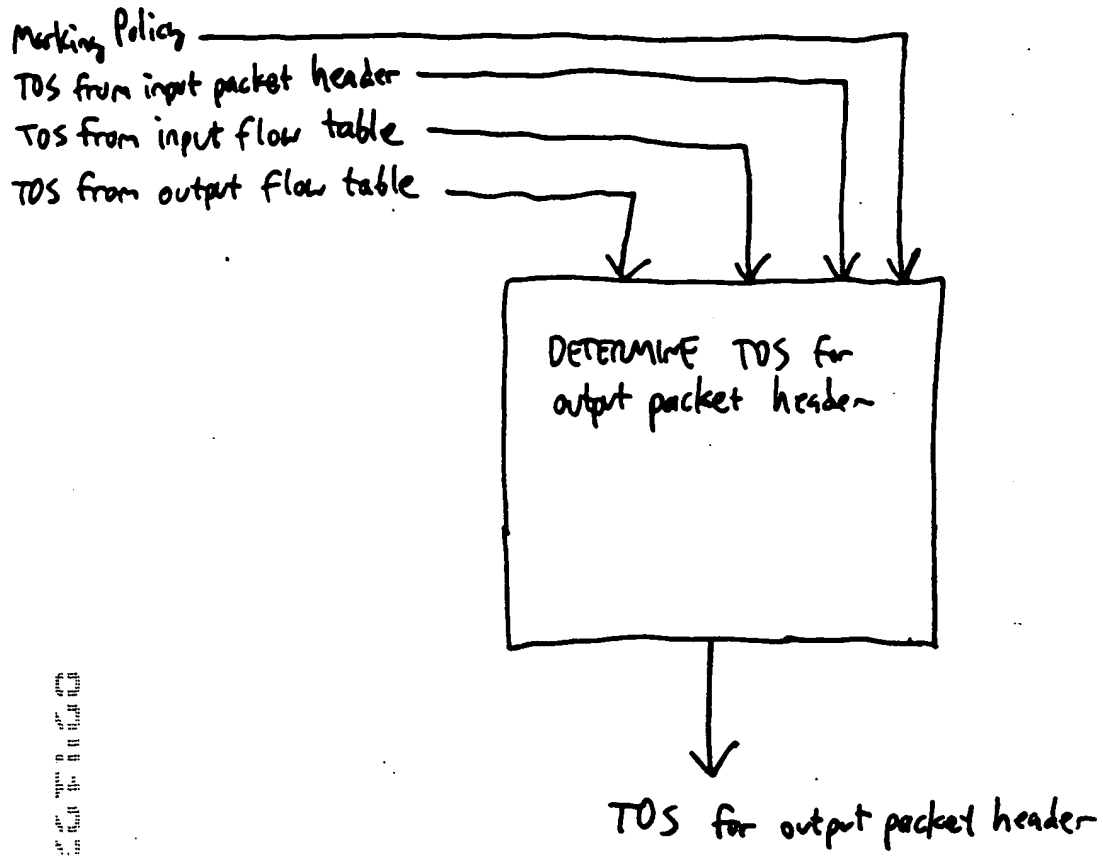


FIGURE 17c

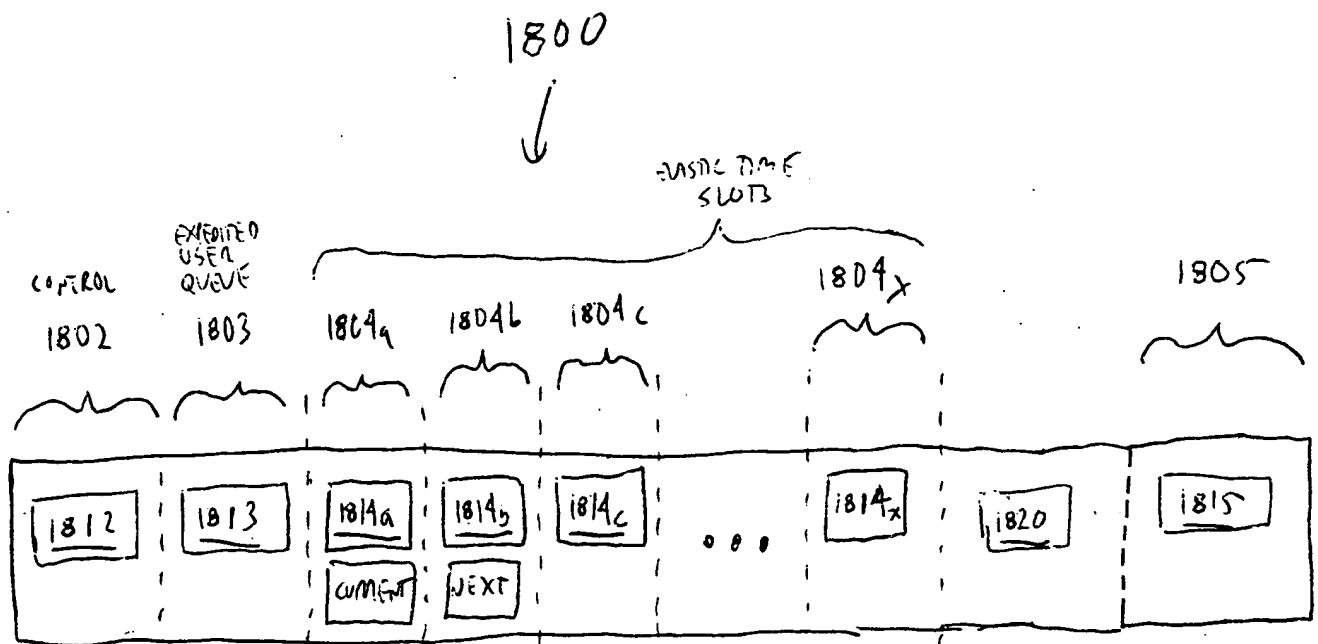


FIGURE 18